EXHIBIT E

Filed: February 28, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR
PRODUCTS, INC.; and MICRON TECHNOLOGY TEXAS LLC,
Petitioners,

v.

NETLIST, INC.,
Patent Owner.

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Case IPR2022-00236
Patent 9,824,035 B2

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PATENT OWNER'S SUR-REPLY

As another example, Petitioners superficially point to various places where write leveling is referred to as an "operation" or is referred to under headings relating to operations or commands. Reply, 3-4. But the claimed "*second memory operation*" as described in the '035 Patent claims and specification cannot be equated to anything referred to as an "operation" or "command" or included in a table with other operations and commands merely by association. Netlist's expert provided extensive, unrebutted testimony regarding why a POSITA would not understand Tokuhiro's write leveling technique to constitute the claimed "*memory operation*," while Petitioners' expert merely summarily concluded that it satisfies the claims and asked the Board to do the same. *Compare* Ex.-2010, ¶¶73-86 *with* Ex.-1003, ¶121.

Petitioners also argue that "regular read and write operations also use . . . NOP and Deselect commands" and thus cannot be distinguished from write leveling. Reply, 4. However, as Dr. Przybylski testified during his deposition, when the SDRAM receives a NOP command during write leveling, "it does nothing." Ex.-1022, 24:14-17, 25:25-26:7 ("The NOP command is a placeholder for doing nothing. So it's a – it's not proactively telling it to do anything."); Ex.-2014, 32 ("[NOP] prevents unwanted commands from being registered during idle or wait states."). The DESELECT command "performs the same function as a No Operation command" and, thus, neither can fairly constitute the claimed "*memory operation.*" *Id.*, 26:6-11. Petitioners do not argue otherwise.

Elsewhere, Petitioners misrepresent Netlist's position. For example, Petitioners concede that "a MRS command is not a '*memory operation*'" but insist that "Netlist admits" that MRS commands "trigger memory operations like write leveling." Reply, 3. This is false, as Netlist expressly argued in its Response that the write leveling procedure that follows any MRS command does not include any "*memory operation*" and is not a "*memory operation*" in its own right. Resp., 20-29.

Petitioners also misrepresent that Netlist argues that JESD79-3A's Simplified State Diagram supports Netlist's position "because 'write leveling' is depicted in connection with an 'idle' state, before the 'activating' state." Reply, 5. But this mischaracterizes Netlist's position. The Simplified State Diagram supports Netlist's position because it shows that the write leveling state is entered before any of the memory banks are activated. *See* Ex.-2014, Fig. 1. In this state, the memory banks are unable to perform read and write commands. *See id.* The Simplified State Diagram also shows that NOP and DESELECT do not cause any actions at all, "*memory operation*" or otherwise. Further, write leveling must be completed before any memory system with a fly-by-topology is capable of reliably performing a write command. Ex.-2014, 7 ("Therefore, DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew"); *id.*, 13 ("The DQS-DQS# delay established through this exercise would **ensure** tDQSS specification") (emphasis added).

Lastly, Petitioners point to claim construction arguments in another proceeding, for a different patent, relating to a different term to allege that Netlist is taking inconsistent positions. Reply, 6. To start, the term at issue there was not, as Petitioners contend, "one or more operations"; it was "one or more **previous** operations." Reply, 6 (emphasis added); Ex.-1023, 4. And the "previous operations" referred to in that claim were "memory read operations," which that specification expressly identified as a "memory operation." Ex.-1023, 4 ("The memory module is operable to perform memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.)").

Petitioners' proof for this claim limitation fails across all Grounds.

B.   Ground 1: Petitioners' proposed combination of Osanai and Tokuhiro does not disclose all limitations of the challenged claims.

    1.   Petitioners fail to provide evidence that any reference discloses or suggests "*logic . . . further configured to . . . control timing of the respective data and strobe signals on the data paths in accordance with the timing information*" as claimed (all claims).

In its Response, Netlist demonstrated Petitioners' failure to allege or show that the proposed combination of Osanai and Tokuhiro discloses "*logic . . . further configured to . . . control timing of the respective data and strobe signals on the data paths in accordance with the timing information.*" Resp., 29-35. Specifically, Netlist established that the Petition never alleged that the proposed combination discloses "*control [of] timing*" on the claimed "*data paths,*" which must be "*for transmitting*

Dated: February 28, 2023   Respectfully submitted,

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